VLSI Design Lab

Lab Module 1: Introduction to the EDA Environment and MOS Characteristics Simulation

Duration: 3 Hours

1. Objective(s):

Upon successful completion of this laboratory session, students will be able to:

- Navigate and effectively operate the core components of the Electronic Design Automation (EDA) tool suite designated for VLSI design (e.g., schematic editor, simulator, waveform viewer).
- Establish and manage a new design project, including proper directory structuring and library association.
- Perform schematic capture of fundamental circuit elements, including placing and wiring MOS transistors and voltage sources.
- Configure and execute basic SPICE (Simulation Program with Integrated Circuit Emphasis) simulations for DC and Transient analysis.
- Simulate and meticulously analyze the fundamental Current-Voltage (I-V) characteristics of both NMOS and PMOS transistors.
- Simulate and analyze the essential Capacitance-Voltage (C-V) characteristics of MOS transistors.
- Extract key transistor parameters such as threshold voltage (Vt) from simulated I-V curves.
- Understand and explain the profound impact of the Width-to-Length (W/L) ratio on MOS transistor electrical characteristics.

2. Theory and Background:

Integrated circuits, the foundation of modern electronics, are built from billions of interconnected transistors. The most prevalent type of transistor used in VLSI is the Metal Oxide Semiconductor (MOS) Field-Effect Transistor (MOSFET). Understanding its fundamental electrical characteristics is paramount for any VLSI designer.

2.1 The MOS Transistor:

The MOS transistor operates as a voltage-controlled switch or current source. Its behavior is primarily governed by the voltages applied to its four terminals: Gate (G), Drain (D), Source (S), and Bulk (B).

- **NMOS (N-channel MOSFET):** Conducts current when a sufficiently positive voltage is applied to its gate, creating an N-type channel between the source and drain. The bulk (substrate) is typically connected to the lowest potential (ground, GND).

- **PMOS (P-channel MOSFET):** Conducts current when a sufficiently negative voltage is applied to its gate (or sufficiently low relative to its source), creating a P-type channel. The bulk (N-well) is typically connected to the highest potential (VDD).

2.2 MOS Transistor Operating Regions:

An understanding of the three main operating regions is critical for designing digital circuits:

- **Cutoff Region:** The transistor is OFF, acting as an open switch. For NMOS, this occurs when VGS < Vt (threshold voltage). For PMOS, when |VGS| < |Vt|.
- **Triode Region (Linear Region):** The transistor is ON and acts like a voltage-controlled resistor. For NMOS, VGS > Vt and VDS < (VGS - Vt). For PMOS, |VGS| > |Vt| and |VDS| < (|VGS| - |Vt|).
- **Saturation Region:** The transistor is ON and acts like a voltage-controlled current source, with drain current relatively independent of VDS. For NMOS, VGS > Vt and VDS >= (VGS - Vt). For PMOS, |VGS| > |Vt| and |VDS| >= (|VGS| - |Vt|).

2.3 I-V (Current-Voltage) Characteristics:

These plots illustrate the relationship between the currents flowing through the transistor (specifically Drain Current, ID) and the voltages applied across its terminals.

- **ID-VDS Curves (Output Characteristics):** Shows ID vs. VDS for different fixed VGS values. These curves clearly delineate the triode and saturation regions.
- **ID-VGS Curves (Transfer Characteristics):** Shows ID vs. VGS for a fixed (typically high) VDS. This curve is used to extract the threshold voltage (Vt), the minimum gate voltage required to turn the transistor on.

2.4 C-V (Capacitance-Voltage) Characteristics:

MOS transistors exhibit various internal capacitances (e.g., gate-to-source Cgs, gate-to-drain Cgd, gate-to-bulk Cgb, and total gate capacitance Cgg). These capacitances are not constant; they vary with the applied terminal voltages and are crucial for determining circuit delay and dynamic power consumption.

- The gate capacitance, in particular, varies significantly as the transistor transitions through cutoff, depletion, and inversion, influencing how quickly the transistor can switch.

2.5 The Width-to-Length (W/L) Ratio:

The physical dimensions of the transistor's channel (Width W and Length L) are critical design parameters. The W/L ratio profoundly influences the transistor's current driving capability (strength) and its associated parasitic capacitances.

- **Current Drive:** A larger W/L ratio (primarily larger W) leads to increased drain current (ID) for a given VGS, meaning the transistor can drive more current and thus switch faster or drive larger loads.

- **Parasitic Capacitance:** A larger W also increases the transistor's internal capacitances, which in turn increases the dynamic power consumption and contributes to signal delays.
- **Trade-offs:** Designers constantly optimize the W/L ratio to balance speed, power, and area requirements for specific applications.

2.6 Electronic Design Automation (EDA) Tools and SPICE Simulation:

EDA tools are specialized software suites used to design, simulate, verify, and lay out integrated circuits. They automate complex processes, significantly improving efficiency and accuracy.

- **Schematic Editor:** A graphical interface for drawing circuits using symbolic components. It translates the schematic into a textual **netlist**.
- **SPICE Simulator:** A powerful engine that takes the netlist and device models (mathematical descriptions of transistors for a specific fabrication process) as input. It then numerically solves the circuit equations to predict voltages and currents, performing various analyses like:
    - **DC Analysis:** Calculates the steady-state operating point (voltages/currents at a fixed input) or sweeps a DC input to show how the circuit responds.
    - **Transient Analysis:** Calculates circuit behavior over time, showing waveforms of voltages and currents, critical for dynamic analysis (delays, switching).
- **Waveform Viewer:** A post-processing tool to visualize and measure quantities from simulation results.

3. Pre-Lab Questions and Preparation:

Students are expected to complete the following before coming to the lab session.

1. **Review MOS Transistor Basics:** Describe the structure of an NMOS and PMOS transistor. What are their four terminals, and what is the typical voltage connection for the bulk terminal in digital CMOS circuits?
2. **Define Operating Regions:** For an NMOS transistor, define the conditions (VGS and VDS relative to Vt) for the cutoff, triode, and saturation regions.
3. **Sketch Expected Curves:** Sketch the expected ID-VDS and ID-VGS characteristic curves for an NMOS transistor. Label the axes and indicate the different operating regions on the ID-VDS plot.
4. **Purpose of W/L Ratio:** Explain why the Width-to-Length (W/L) ratio is a crucial parameter in MOS transistor design. How does increasing W typically affect ID and gate capacitance?
5. **Role of SPICE:** Briefly explain the primary purpose of SPICE simulation in VLSI design. Differentiate between DC and Transient analysis.
6. **Lab Environment Setup:** Ensure you have your login credentials ready for the lab computing environment. If any specific software needs to be pre-downloaded or configured on your personal machine for remote access, ensure this is done.

4. Procedure/Experimental Steps:

Follow these steps carefully to complete the lab experiment. Document all your actions, observations, and generated plots in your lab notebook or report.

4.1 Task 1: Introduction to the EDA Environment and Project Setup

1. **Login to the Lab Workstation/Server:**
    - Power on the workstation or open your terminal/SSH client.
    - Enter your provided username and password to log into the Linux environment.
2. **Navigate and Create Your Project Directory:**
    - Open a terminal window.
    - Navigate to your home directory: `cd ~`
    - Create a dedicated directory for this lab: `mkdir -p vlsi_lab/lab1_mos_char`
    - Change into your new lab directory: `cd vlsi_lab/lab1_mos_char`
3. **Launch the Main EDA Design Environment:**
    - At the terminal, launch the primary design tool (e.g., for Cadence Virtuoso, type `virtuoso &` and press Enter). The `&` symbol runs the process in the background, keeping your terminal free.
    - Familiarize yourself with the main design window, which typically includes menus, toolbars, and a design hierarchy browser.
4. **Create a New Library and Cell View:**
    - From the main EDA window, use the menu options (e.g., File > New > Library) to create a new library for your designs (e.g., `mylib`). Attach it to the appropriate technology file (provided by your instructor, e.g., `gpdk_180nm` or similar).
    - Within your new library, create a new cell view for your NMOS test bench (e.g., File > New > Cell View, Library: `mylib`, Cell Name: `nmos_iv_cv_tb`, View: `schematic`). This will open the schematic editor.

4.2 Task 2: Schematic Capture of NMOS I-V/C-V Test Bench

1. **Place NMOS Transistor:**
    - Locate the "Instance" placement tool (often an icon or from menu: Create > Instance).
    - Browse the technology library (e.g., `gpdk_180nm` if using Cadence) to find the NMOS transistor (often named `nmos` or `nfet`).
    - Place a single NMOS transistor on the schematic canvas.
    - **Set Parameters:** Select the NMOS transistor. Modify its properties (often by pressing 'Q' or double-clicking). Set typical dimensions:
        - Width (W): e.g., `500n` (500 nanometers) or `0.5u` (0.5 micrometers)
        - Length (L): e.g., `180n` (180 nanometers) or `0.18u` (0.18 micrometers)
        - Number of fingers (if applicable): `1`
        - Multiplier (if applicable): `1`
2. **Place Voltage Sources:**
    - Place three independent DC voltage sources (`vdc` from `analogLib` or equivalent) for VGS, VDS, and VBS (Bulk voltage for NMOS).
    - Place a Ground symbol (`gnd` from `analogLib`).
3. **Wire the Test Bench:**

- Connect the Source terminal of the NMOS to a dedicated wire/net (e.g., "src").
- Connect the Drain terminal of the NMOS to a dedicated wire/net (e.g., "drn").
- Connect the Gate terminal of the NMOS to a dedicated wire/net (e.g., "gate").
- Connect the Bulk terminal of the NMOS directly to the Ground (gnd) symbol.
- Connect the positive terminal of one vdc to "gate" and its negative terminal to "src" (this is your VGS source).
- Connect the positive terminal of another vdc to "drn" and its negative terminal to "src" (this is your VDS source).
- Connect the third vdc to define the bulk voltage, connecting its positive terminal to "src" and negative to "bulk" (if not direct ground connection). For this lab, ensure bulk is at ground reference.
- Connect the gnd symbols from all voltage sources to a common ground net.
- Place output current probes if available (e.g., i_probe to measure ID from drain).

4. **Check and Save:**
   - Perform a "Check and Save" (often a toolbar button or Design > Check and Save) to ensure your schematic is electrically valid. Resolve any warnings or errors.

4.3 Task 3: Simulating NMOS I-V Characteristics (ID-VDS)

1. **Launch the Simulator:**
   - From the schematic window, launch the simulation environment (e.g., Launch > ADE L or similar).
2. **Select Analysis Type:**
   - Add a "DC Analysis" (Analyses > Choose Analyses... > dc).
   - **Set DC Sweep Parameters:**
     - Select "Component Parameter" for the sweep variable.
     - Choose the VDS voltage source (e.g., VDS_source).
     - Set Start Value: 0V
     - Set Stop Value: VDD (e.g., 1.8V or 3.3V from technology file)
     - Set Step Type: Linear (or Automatic), Number of Steps: sufficient (e.g., 100 points).
     - **Enable Parameter Sweep (for VGS):** Go to the "Design Variables" or "Parametric Analysis" section.
     - Define VGS_val as a variable linked to your VGS source value.
     - Set VGS_val to sweep from 0V to VDD (e.g., 1.8V) with a step size (e.g., 0.2V or 0.4V).
3. **Select Outputs to Plot:**
   - In the schematic, select the Drain Current (ID) of the NMOS transistor (often by clicking on the drain terminal, or using a current probe).
   - Ensure the output variable is added to the simulation's output list.
4. **Run Simulation:**
   - Start the simulation (e.g., "Netlist and Run" button).
   - The waveform viewer will launch and display the ID-VDS curves.
5. **Analyze and Document:**

- Observe the family of ID-VDS curves. Identify the cutoff, triode, and saturation regions for different VGS values.
- Capture a screenshot of your ID-VDS plots.

4.4 Task 4: Simulating NMOS I-V Characteristics (ID-VGS) and Vt Extraction

1. **Modify Simulation Setup:**
   - Return to the simulation environment. Keep the "DC Analysis" enabled.
   - **Change Sweep Parameter:** Now, sweep the `VGS` voltage source (e.g., `VGS_source`) from `0V` to `VDD`.
   - **Fix VDS:** Set the `VDS` voltage source to a fixed value (e.g., `VDD` or a value sufficient to put the transistor into saturation).
   - Ensure the output to plot is still `ID` of the NMOS.
2. **Run Simulation:** Execute the simulation.
3. **Analyze and Extract Vt:**
   - Observe the ID-VGS curve.
   - **Method 1 (Visual Estimation):** Visually estimate the VGS value where the drain current begins to significantly increase from zero.
   - **Method 2 (Linear Extrapolation - if supported by viewer):** Many waveform viewers have tools to draw a tangent line to the steepest part of the ID-VGS curve and find its X-axis intercept, which gives a more precise Vt.
   - Document the extracted threshold voltage.
   - Capture a screenshot of your ID-VGS plot and indicate your Vt extraction method.

4.5 Task 5: Simulating NMOS C-V Characteristics (Cgg vs. VGS)

1. **Modify Test Bench (if needed for C-V setup):**
   - Ensure your NMOS schematic is set up for C-V measurement (some tools require specific AC sources or test configurations for capacitance extraction). Typically, you'll need to apply DC biases and then a small AC signal.
2. **Select Analysis Type:**
   - Add an "AC Analysis" (Analyses > Choose Analyses... > ac).
   - **Set AC Sweep Parameters:**
     - Sweep Type: `Frequency` (e.g., single point at `1M Hz` or `1k Hz`, very low frequency for quasi-static C-V).
     - Sweep Range: Set start and stop frequencies (e.g., `1kHz` to `1kHz` for single point).
     - **Enable Parameter Sweep (for VGS):** Go to the "Design Variables" or "Parametric Analysis" section.
     - Sweep the `VGS` voltage source (e.g., `VGS_source`) from `0V` to `VDD` (e.g., `1.8V`).
3. **Select Outputs to Plot:**
   - Select the total gate capacitance (`Cgg`) of the NMOS transistor. The specific expression might be `deriv(ID(MN0))` or a dedicated capacitance probe, depending on the tool.
4. **Run Simulation:** Execute the simulation.

5. **Analyze and Document:**
    - Observe the Cgg vs. VGS curve.
    - Explain the shape of the curve in terms of accumulation, depletion, and inversion regions.
    - Capture a screenshot of your C-V plot.

4.6 Task 6: PMOS Transistor Characteristics Simulation

1. **Create New Cell View for PMOS:**
    - Create a new schematic cell view for your PMOS test bench (e.g., `pmos_iv_cv_tb`).
2. **Schematic Capture for PMOS:**
    - Place a single PMOS transistor (`pmos` or `pfet`).
    - **Set Parameters:** Use similar W/L dimensions as the NMOS (e.g., `W=0.5u`, `L=0.18u`). *Note: For later inverter design, PMOS W is often larger than NMOS W.*
    - Place three independent DC voltage sources for VGS, VDS.
    - Connect the Bulk terminal of the PMOS to the highest potential (`VDD`) symbol.
    - Wire the test bench appropriately, similar to the NMOS, but keeping in mind PMOS operates with negative VGS/VDS relative to VDD for current flow.
        - Example: Source to `VDD_source`, Gate to `VGS_source`, Drain to `VDS_source`. The `VGS_source` and `VDS_source` will typically be swept from `VDD` downwards to `0V`.
3. **Simulate PMOS I-V Characteristics (ID-VDS and ID-VGS):**
    - Repeat steps 4.3 and 4.4 for the PMOS transistor. Remember that PMOS current flows when VGS is below Vt (negative Vt, or VGS closer to 0V than VDD).
    - Observe and document the differences in curve shapes and operating regions compared to the NMOS.
    - Extract the threshold voltage (`Vt`) for the PMOS transistor (it will be a negative value or close to 0V relative to VDD).
    - Capture screenshots of your PMOS I-V plots.
4. **Simulate PMOS C-V Characteristics (Cgg vs. VGS):**
    - Repeat step 4.5 for the PMOS transistor.
    - Observe and document the C-V curve, noting how it differs from NMOS due to opposite carrier types and voltage dependencies.
    - Capture a screenshot of your PMOS C-V plot.

4.7 Task 7: Impact of W/L Ratio (Comparative Analysis)

1. **Create New Schematic (e.g., `nmos_wl_impact_tb`):**
    - Copy your `nmos_iv_cv_tb` schematic into a new cell view.
2. **Parametric Simulation Setup:**
    - Modify the NMOS transistor instance. Instead of a fixed W, define a design variable (e.g., `my_W`) for its width.

    - In the simulation environment, set up a "Parametric Analysis" to sweep `my_W` through several values (e.g., `0.5u`, `1u`, `2u`).
    - Run the ID-VDS or ID-VGS simulation with this parametric sweep.
3. **Analyze and Document:**
    - Observe how the ID current changes dramatically with varying `W`.
    - Observe how the Cgg capacitance changes with varying `W`.
    - Quantify the change in current drive as W is doubled.
    - Capture screenshots showing the family of curves for different W values.

5. Post-Lab Questions and Analysis:

Answer the following questions comprehensively in your lab report, incorporating your simulation results and observations.

1. **EDA Environment Reflection:** Describe your initial experience with the EDA tool. What were the most challenging aspects of navigation or schematic capture, and how did you overcome them?
2. **NMOS vs. PMOS Characteristics:** Compare and contrast the ID-VGS and ID-VDS characteristics of the NMOS and PMOS transistors. Explain the differences in their operating principles and why their curves appear "mirrored."
3. **Threshold Voltage:** What were the extracted threshold voltages (Vt) for your simulated NMOS and PMOS transistors? Discuss the significance of the threshold voltage in circuit operation.
4. **Operating Regions Explained:** Based on your ID-VDS plots, clearly identify and explain the cutoff, triode, and saturation regions for both NMOS and PMOS. How would you determine which region a transistor is in given its terminal voltages?
5. **C-V Curve Interpretation:** Explain the shape of the C-V curves you obtained for both NMOS and PMOS. How does the gate capacitance change as the gate voltage sweeps from below to above the threshold voltage? Why is this significant for circuit performance?
6. **Impact of W/L Ratio:** Based on your simulation results from Task 7, quantitatively describe the impact of increasing the transistor's width (W) on its current driving capability and its associated gate capacitance. Discuss the fundamental design trade-offs involved when choosing the W/L ratio for a transistor (e.g., speed, power, area).
7. **Importance of Simulation:** Reflect on why simulating individual transistor characteristics is a crucial first step in VLSI design. What insights did you gain that would be difficult to obtain from purely theoretical calculations?

6. Deliverables:

Your lab report should include the following sections and content:

1. **Title Page:** Your name, student ID, course name, lab number, date of submission.
2. **Objectives:** Copy the objectives from this lab module.
3. **Pre-Lab Questions:** Your answers to the pre-lab questions.
4. **Procedure Summary:** A brief description of the steps you followed for each task.
5. **Simulation Results and Analysis (Core of the Report):**

    - Clearly labeled screenshots of all required plots:
        - NMOS ID-VDS characteristics (Task 3).
        - NMOS ID-VGS characteristics with Vt extraction indication (Task 4).
        - NMOS Cgg-VGS characteristics (Task 5).
        - PMOS ID-VDS characteristics (Task 6).
        - PMOS ID-VGS characteristics with Vt extraction indication (Task 6).
        - PMOS Cgg-VGS characteristics (Task 6).
        - NMOS ID-VDS or ID-VGS characteristics showing the impact of W variations (Task 7).
    - Detailed analysis for each plot, explaining what the graph shows, relevant values extracted (e.g., Vt), and its significance.
6. **Post-Lab Questions:** Your comprehensive answers to all post-lab questions.
7. **Conclusion:** A concise summary of what you learned in the lab, including key takeaways regarding MOS transistor characteristics and the use of EDA tools.